

P-Channel Enhancement-Mode Vertical DMOS FET

Features

- ► Low threshold (-2.4V max.)
- ▶ High input impedance
- ► Low input capacitance (95pF typical)
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Part Number	Package Option	Packing		
TP0604N3-G	3-Lead TO-92	1000/Bag		
TP0604N3-G P002				
TP0604N3-G P003				
TP0604N3-G P005	3-Lead TO-92	2000/Reel		
TP0604N3-G P013				
TP0604N3-G P014				
TP2404NW	Die in wafer form			
TP2404NJ	Die on adhesive tape			
TP2404ND	Die in waffle pack			

For packaged products, -G indicates package is RoHS compliant ('Green'). TO-92 taping specifications and winding styles per EIA-468 Standard. Devices in Wafer / Die form are RoHS compliant ('Green'). Refer to Die Specification VF57 for layout and dimensions.

Absolute Maximum Ratings

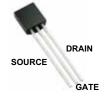
Parameter	Value
Drain-to-source voltage	BV _{DSS}
Drain-to-gate voltage	BV _{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Product Summary

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	l _{D(ON)} (min) (A)	V _{GS(th)} (max) (V)	
-40	2.0	-2.0	-2.4	

Pin Configuration



TO-92 (N3)

Product Marking



YY = Year Sealed WW = Week Sealed ____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I _D (continuous) [†] (A)	I _D (pulsed) (A)	Power Dissipation @T _A = 25°C (W)	θ _{ja} (°C/W)	_{DR}	I _{DRM} (A)
TO-92	-0.43	-4.2	0.74	132	-0.43	-4.2

Notes:

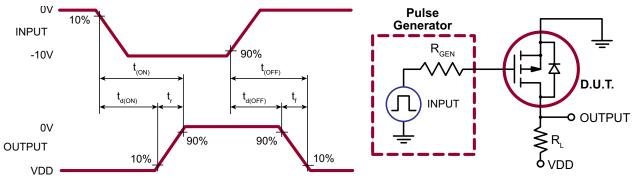
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Тур	Max	Units	Conditions	
BV _{DSS}	Drain-to-source breakdown voltage	-40	-	-	V	$V_{GS} = 0V, I_{D} = -2.0 \text{mA}$	
$V_{\rm GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}$, $I_D = -1.0$ mA	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with temperature	-	-3.0	-4.5	mV/°C	$V_{GS} = V_{DS}$, $I_{D} = -1.0$ mA	
I _{GSS}	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
		-	-	-10	μΑ	$V_{GS} = 0V, V_{DS} = Max Rating$	
I _{DSS}	Zero gate voltage drain current	-	-	-1.0	mA	$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0V$, $T_{A} = 125$ °C	
	ON-state drain current	-0.4	-0.6	-	Α	$V_{GS} = -5.0V, V_{DS} = -20V$	
D(ON)	ON-State drain current	-2.0	-3.3	-	A	$V_{GS} = -10V, V_{DS} = -20V$	
D	Static drain to source on state registance	-	2.0	3.5	Ω	$V_{GS} = -5.0V, I_{D} = -250mA$	
R _{DS(ON)}	Static drain-to-source on-state resistance		1.5	2.0	12	$V_{GS} = -10V, I_{D} = -1.0A$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with temperature	-	-	1.2	%/°C	$V_{GS} = -10V, I_{D} = -1.0A$	
G _{FS}	Forward transductance	400	600	-	mmho	$V_{DS} = -20V, I_{D} = -1.0A$	
C _{ISS}	Input capacitance	-	95	150		$V_{GS} = 0V$	
C _{oss}	Common source output capacitance	-	85	120	pF	$V_{DS} = -20V$,	
C _{RSS}	Reverse transfer capacitance	-	35	60		f = 1.0MHz	
t _{d(ON)}	Turn-on delay time	-	5.0	8.0			
t _r	Rise time	-	7.0	18	ns	$V_{DD} = -20V,$ $I_{D} = -1.0A,$	
t _{d(OFF)}	Turn-off delay time	-	10	15	115	$R_{GEN} = 25\Omega$	
t	Fall time	-	6.0	19		GEN 2012	
$V_{_{\mathrm{SD}}}$	Diode forward voltage drop	-	-1.3	-2.0	V	$V_{GS} = 0V, I_{SD} = -1.5A$	
t _{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -1.5A$	

Notes:

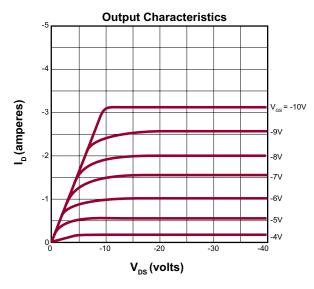
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300µs pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

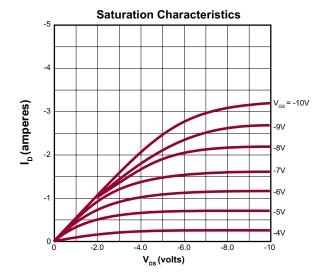
Switching Waveforms and Test Circuit

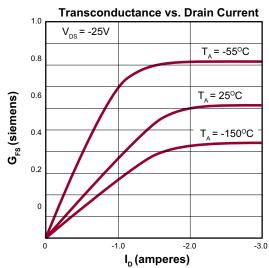


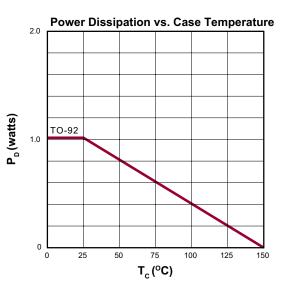
[†] I_D (continuous) is limited by max rated T_i .

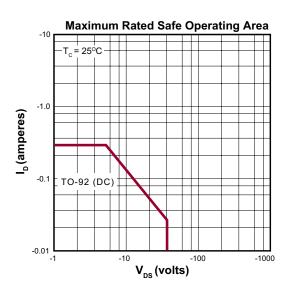
Typical Performance Curves

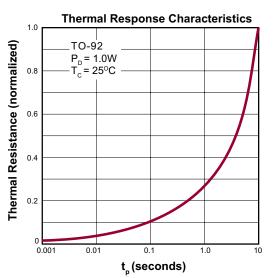




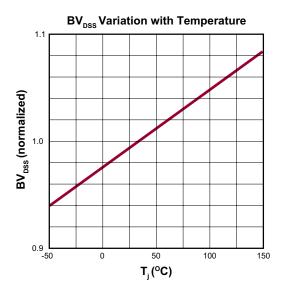


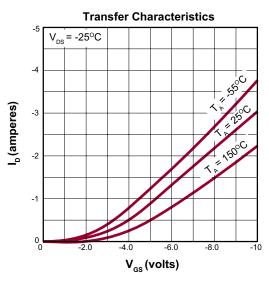


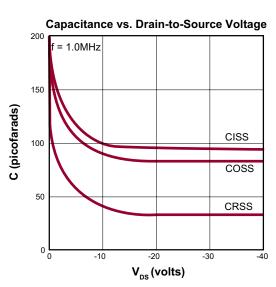


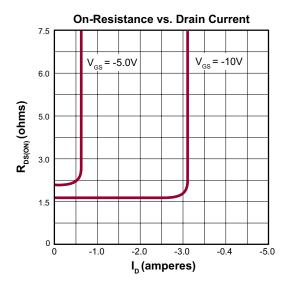


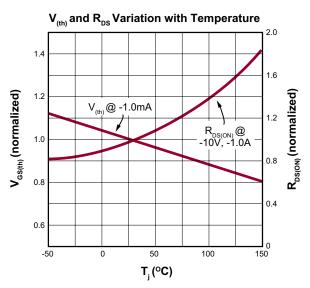
Typical Performance Curves (cont.)

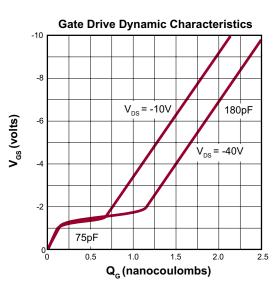




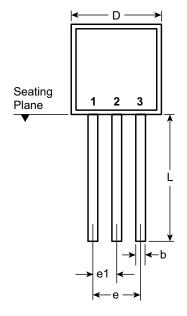


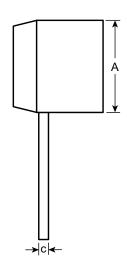






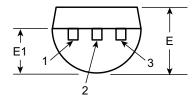
3-Lead TO-92 Package Outline (N3)





Front View

Side View



Bottom View

Symb	ool	Α	b	С	D	E	E1	е	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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^{*} This dimension is not specified in the JEDEC drawing.

[†] This dimension differs from the JEDEC drawing.